Docket No.: 1081.1190 Serial No. 10/780,607

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 2, 4, 8, AND 9 in accordance with the following:

1. (CURRENTLY AMENDED) A bus connection circuit, which is connected via a bus to a bridge circuit having a plurality of pre-fetch buffers for pre-fetching of data from an external device, and which receives data from said pre-fetch buffers after assertion of a request, comprising:

a plurality of request queues;

an arbiter which performs arbitration of the requests of said plurality of request queues; and

a bus interface portion which outputs request signals indicating ~~the~~ allocation of said pre-fetch buffers corresponding to requests arbitrated by said arbiter, and which receives corresponding grant signals from said bridge circuit~~.~~, said bus interface portion being connected via said bus and a plurality of request lines, corresponding to the allocation of said pre-fetch buffers to said bridge circuit, and outputs respective request signals to said request lines corresponding to said requests arbitrated by said arbiter.

2. (CURRENTLY AMENDED) The bus connection circuit according to Claim 1, wherein said bus interface portion releases said bus according to said request signal upon reception of a retry response from said bridge circuit prompted by said request signal, and outputs to said ~~bus~~ request line a request signal indicating the allocation of other pre-fetch buffers.

3. (ORIGINAL) The bus connection circuit according to Claim 2, wherein said request queues give priority to and assert an initial read request over a read request corresponding to said retry response.

4. (CURRENTLY AMENDED) The bus connection circuit according to Claim 2, wherein said request queues have a register which sets ~~the~~ a time, from receipt of said retry response until assertion of the read request corresponding to said retry response.

5. (ORIGINAL) The bus connection circuit according to Claim 1, further having an internal circuit which issues read requests to said plurality of request queues.

6. (ORIGINAL) The bus connection circuit according to Claim 1, wherein said request is a read request to memory via said bridge circuit.

7. (ORIGINAL) The bus connection circuit according to Claim 1, wherein said bus is a PCI bus.

8. (CURRENTLY AMENDED) A bus connection system, comprising:

a bridge circuit with a plurality of pre-fetch buffers to pre-fetch data from memory; and

a bus connection circuit, which is connected to said bridge circuit via a bus, and which, after assertion of a request, receives data from said pre-fetch buffers,

wherein said bus connection circuit comprises:

a plurality of request queues;

an arbiter which performs arbitration of the requests of said plurality of request queues; and

a bus interface portion which outputs request signals indicating ~~the~~ allocation of said pre-fetch buffers corresponding to requests arbitrated by said arbiter, and which receives corresponding grant signals from said bridge circuit~~.~~, said bus interface portion being connected via said bus and a plurality of request lines, corresponding to the allocation of said pre-fetch buffers, to said bridge circuit, and outputting request signals to said request line corresponding to said request arbitrated by said arbiter.

9. (CURRENTLY AMENDED) The bus connection system according to Claim 8, wherein said bus interface portion of said bus connection circuit releases said bus according to said request signal upon reception of a retry response from said bridge circuit prompted by said request signal, and outputs to said ~~bus~~ request line a request signal indicating the allocation of another pre-fetch buffers.

10. (ORIGINAL) The bus connection system according to Claim 9, wherein said request queues of said bus connection circuit give priority to and assert an initial read request over a read request corresponding to said retry response.

11. (ORIGINAL) The bus connection system according to Claim 9, wherein said request queues of said bus connection circuit have a register which sets the time from receipt of said retry response until assertion of the read request corresponding to said retry response.

12. (ORIGINAL) The bus connection system according to Claim 8, wherein said bus connection circuit further comprises an internal circuit which issues read requests to said plurality of request queues.

13. (ORIGINAL) The bus connection system according to Claim 8, wherein said request is a read request to memory via said bridge circuit.

14. (ORIGINAL) The bus connection system according to Claim 8, wherein said bus is a PCI bus.

15. (ORIGINAL) The bus connection system according to Claim 8, wherein said bridge circuit assigns corresponding pre-fetch buffers in response to said request signals, outputs retry responses to said bus connection circuit, and outputs read requests to said memory.

16. (ORIGINAL) The bus connection system according to Claim 15, wherein said bridge circuit examines corresponding pre-fetch buffers in response to request signals for said retry responses, and transfers data in said pre-fetch buffers to said bus connection circuit.